UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/059,014	01/29/2002	Chong Lee	174/211	5565

36981 7590 03/03/2006

FISH & NEAVE IP GROUP
ROPES & GRAY LLP
1251 AVENUE OF THE AMERICAS FL C3
NEW YORK, NY 10020-1105

EXAMINER	
WANG, TED M	

ART UNIT	PAPER NUMBER
2634	

DATE MAILED: 03/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/059,014	LEE ET AL.	
	Examiner	Art Unit	
	Ted M. Wang	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,6-19 and 22-26* is/are rejected.

7)☒ Claim(s) *4, 5, 20, 21, and 27-37* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 April 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's amendments and arguments, filed 12/08/2005, with respect to the rejection(s)of claim(s) 1-3, 5-19, and 21-26 under 35 U.S.C. 112 second paragraph, 35 U.S.C. 102(e), and 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Tanji et al. (US 6,307,906).

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-3, 6-10, 16-19, and 22-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al. (US 6,266,799) in view of Tanji et al. (US 6,307,906).

- With regard claim 1, Lee et al. discloses Circuitry for using a reference clock signal to extract data from a data signal (Fig.1 and Fig.2 element 110a, and column 4 line 40 – column 5 line 61), the data signal having a data rate that is twice the reference clock signal frequency (column 7 lines 42-51), comprising:

  first circuitry (Fig.3 element 304) configured to derive from the reference clock signal (Fig.3 element 204) first and second phase-shifted versions of the

reference clock signal (Fig.3 elements UP and DOWN, 306, and 308 and 310 OUTPUT Φ_0-Φ_3) that are respectively synchronized with transitions in level of the data signal (Fig.5 elements ck0 and clk3, column 5 line 40 – column 6 line 4, and column 7 lines 9-42);

second circuitry configured to sample the data signal (Fig.3 elements 302 and 310) in a predetermined phase relationship (Fig.3 elements Φ_0-Φ_3 to the first phase-shifted version in order to produce a first partial stream of data extracted from the data signal (column 2 lines 18-65, and column 11 line 59 – column 12 line 19); and

third circuitry configured to sample the data signal (Fig.3 elements 302 and 310) in a predetermined phase relationship (Fig.3 elements Φ_0-Φ_3) to the second phase-shifted version in order to produce a second partial stream of data extracted from the data signal (column 2 lines 18-65, and column 11 line 59 – column 12 line 19).

Lee et al. discloses all of the subject matter as described in the above paragraph except for specifically teaching first circuitry configured to derive from the reference clock signal first and second phase-shifted versions of the reference clock signal that are respectively synchronized with oppositely polarized transitions in level of the data signal.

However, Tanji et al. teaches that first circuitry Fig.1 elements 14 and 18, Fig.4A and 4B) configured to derive from the reference clock signal first and second phase-shifted versions of the reference clock signal (Fig.4A and 4B) that

are respectively synchronized with oppositely polarized transitions in level of the data signal (column 3 lines 14-44).

It is desirable to have a circuitry configured to derive from the reference clock signal first and second phase-shifted versions of the reference clock signal that are respectively synchronized with oppositely polarized transitions in level of the data signal. The reason for this is that the phase detector is provided for each data input channel. The phase detector determines a phase difference between the data output and the clock signal for each data input channel. The single clock averages the phase differences for all of the data input channels and determines an average data center for all of the data input channels so that the multiple-channel clock and data recovery scheme that is capable of outputting the single clock signal to re-time all of the multiple channel data and that is thereby able to reduce the jitter and channel crosstalk that can occur with multiple clocks (column 1 lines 40-44 and column 2 lines 54-67). Therefore, It would have been obvious to one of ordinary skill in the art at the time of the invention was made to include the circuitry as taught by Tanji et al. to replace the transition detect and lead-lag decision circuit 304 of Lees' so as to reduce the jitter and channel crosstalk that can occur with multiple clocks.

- With regard claim 2, Lee et al. further discloses fourth circuitry configured to produce a plurality of more than two phase-shifted candidate versions of the reference clock signal (Fig.3 element 310 OUTPUT Φ_0-Φ_3 and column 5 line 52 – column 6 line 25).

- With regard claim 3, Lee et al. further discloses

  fifth circuitry configured to select from the candidate versions first and second candidate versions that are most nearly in phase with transitions in the level of the data signal having a first polarity (Fig.3 element 310 output $\Phi_0 - \Phi_3$, Fig.5 elements clk0 and clk3, and column 5 line 40 – column 6 line 43, and column 7 lines 9-51); and

  sixth circuitry configured to select from the candidate versions third and fourth candidate versions that are most nearly in phase with transitions in the level of the data signal having a second polarity (Fig.3 element 310 output $\Phi_0 - \Phi_3$, Fig.5 elements clk0 and clk3, and column 5 line 40 – column 6 line 43, and column 7 lines 9-51).

- With regard claim 6, Lee et al. further discloses first multi-stage shift register circuitry (Fig.4a elements 402a-402d and column 6 line 44 –column 7 line 8) having a data input terminal (Fig.4A element 400 INPUT DATA and /DATA) to which the first partial data stream is applied (Fig.4a element serial IN (NRZ) data), the first shift register circuitry being configured to shift in data from its input terminal in a predetermined phase relationship to the first phase-shifted version (Fig.4a elements $\Phi_0 - \Phi_3$ and clk0 – clk3).

- With regard claim 7, Lee et al. further discloses first shift register reading circuitry configured to read out in parallel the contents of multiple stages of the first shift register circuitry (Fig.2 element 206, Fig.3 and 4a elements D0 – D3, and column 5 lines 48-61).

- With regard claim 8, Lee et al. further discloses wherein the first shift register reading circuitry is configured to operate in a predetermined phase relationship to the first phase-shifted version (Fig.3 element 310 output $\Phi_0 - \Phi_3$, Fig.5 elements clk0 and clk3, and column 5 line 40 – column 6 line 43, and column 7 lines 9-51).
- With regard claim 9, Lee et al. further discloses wherein the first shift register reading circuitry is further configured to operate in response to only a selected fraction of cycles of the first phase-shifted version (column 7 lines 42-51).
- With regard claim 10, Lee et al. further discloses the circuitry defined the fraction is programmably selectable (Fig.3 element 310 and column 6 lines 1-15).
- With regard claim 16, which is a method claim related to claim 1, all limitation is contained in claim 1. The explanation of all the limitation is already addressed in the above paragraph.
- With regard claim 17, which is a method claim related to claim 2, all limitation is contained in claim 2. The explanation of all the limitation is already addressed in the above paragraph.
- With regard claim 18, Lee et al. further discloses the phase shifts of the candidate versions equally divide among them a cycle of the reference clock signal (Fig.3 element 310 output $\Phi_0 - \Phi_3$, Fig.5 elements clk0 and clk3, and column 5 line 40 – column 6 line 43, and column 7 lines 9-51, and column 7 lines 42-51). All other limitation is contained in claim 17. The explanation of all the limitation is already addressed in the above paragraph.

- With regard claim 19, which is a method claim related to claim 3, all limitation is contained in claim 3. The explanation of all the limitation is already addressed in the above paragraph.
- With regard claim 22, which is a method claim related to claim 6, all limitation is contained in claim 6. The explanation of all the limitation is already addressed in the above paragraph.
- With regard claim 23, which is a method claim related to claim 7, all limitation is contained in claim 7. The explanation of all the limitation is already addressed in the above paragraph.
- With regard claim 24, Lee et al. further discloses operation phase locked loop circuitry to produce the reference clock signal (column 3 lines 1-13, Fig.2 element 204, and column 11 lines 11-24).
- With regard claim 25, Lee et al. further discloses an apparatus for receiving an information signal which includes data information having clock information for the data information embedded in the data information comprising:

  first input circuitry configured to receive the information signal (Fig.2 element Data/ Data bar);

  second input circuitry configured to receive a reference clock signal having a reference frequency which is related to a frequency of the clock information by a predetermined scale factor (Fig.2 element 110a input circuit to receive signals from element 204);

reference clock signal processing circuitry (Fig.2 element 110a) configured to use the information signal and the reference clock signal to produce two recovered clock signals, where each recovered clock signal has a respective one of two shifted phases (Fig.3 elements 110a, 310 output $\Phi_0 - \Phi_3$, Fig.5 elements clk0 and clk3, and column 5 line 40 – column 6 line 43, and column 7 lines 9-51), each of which corresponds to a phase of the clock information, and where each recovered clock signal has a frequency that is half a frequency of the clock information (column 7 lines 42-51); and

data recovery circuitry configured to use the two recovered clock signals and the information signal to produce two retimed data output signals indicative of the data information in the information signal (Fig.3 elements 302-310 and column 5 line 62 – column 6 line 43).

All other limitation is contained in claim 1. The explanation of all the limitation is already addressed in the above paragraph.

- With regard claim 26, Lee et al. further discloses first phase locked loop circuitry (Fig.3 element 204 and column 11 lines 11-24) configured to use the reference clock signal and the scale factor to produce a plurality of candidate further reference clock signals (Fig.3 element 310 and output $\Phi_0 - \Phi_3$ and Fig.5 elements clk0-clk3, column 7 lines 42-51, and column 5 line 40 – column 6 line 43, and column 7 lines 9-51), each further reference clock signal having a frequency that is half a frequency of the clock information and having a phase which is different from the phases of all the other candidate further reference

clock signals (Fig.3 element 310 and output $\Phi_0 - \Phi_3$ and Fig.5 elements clk0-clk3, column 7 lines 42-51, and column 5 line 40 – column 6 line 43, and column 7 lines 9-51).

4. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al. (US 6,266,799) and Tanji et al. (US 6,307,906) as applied to claim 1 above, and further in view of Li et al. (US 6,693,985).

- With regard claim 11, Lee et al. and Tanji et al. disclose all of the subject matter as described in the above paragraph except for specifically teaching a Programmable logic device circuitry to implement the clock and data recovery circuit.

  However, Li et al. teaches that a Programmable logic device circuitry to implement a clock and data recovery circuit (column 7 line 58 – column 8 line 21).

  It is desirable to include a Programmable logic device circuitry to implement a clock and data recovery circuit. The reason for this is if the variety of discrete circuitries of clock and data recovery circuit is implemented into a PLD, the circuit complexity and circuit board size can be reduced so that the system cost can be reduced. Therefore, It would have been obvious to one of ordinary skill in the art at the time of the invention was made to include the apparatus as taught by Li et al. in which, having a Programmable logic device circuitry to implement the clock and data recovery circuit, into Lees' data/clock recovery circuitry so as to reduce the total system cost.

5. Claims 12-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al. (US 6,266,799) and Tanji et al. (US 6,307,906) and Li et al. (US 6,693,985) as applied to claim 11 above, and further in view of Wang et al. (US 6,292,116).

- With regard claim 12, Lee et al., Tanji et al., and Li et al. disclose all of the subject matter as described in the claim 11 except for specifically teaching

  a) processing circuitry; and

  b) a memory coupled to said processing circuitry.

  However, Wang et al. further teaches a processing circuitry (Fig.1 element 101) and a memory coupled to said processing circuitry (Fig.1 element 105).

  It is desirable to include a processing circuitry and a memory coupled to said processing circuitry in a board. The reason for this is if the memory coupled to said processing circuitry, the programmable and operational execution software can be stored so that the external control circuitry can be eliminated and it reduce the system cost. Therefore, It would have been obvious to one of ordinary skill in the art at the time of the invention was made to include the apparatus/method as taught by Wang et al. in which, having a processing circuitry and a memory coupled to said processing circuitry, into Lee et al. and Lis' data/clock recovery circuitry so as to reduce the total system cost.

- With regard claims 13-15, Lee et al., Tanji et al., and Li et al. disclose all of the subject matter as described in the claim 11 except for specifically teaching the PLD, the processing circuitry, and the memory will be mounted on a printed circuit board.

However, Wang et al. further teaches the PLD, the processing circuitry, and the memory will be mounted on a printed circuit board (column 3 lines 19-40).

It is desirable to mount the PLD, the processing circuitry, and the memory on a printed circuit board for operation in order to reduce the extra wiring and external interface connection so that the system reliability can be improved. Therefore, It would have been obvious to one of ordinary skill in the art at the time of the invention was made to mount the PLD, the processing circuitry, and the memory on a printed circuit board as taught by Wang et al. into Lee et al. and Lis' data/clock recovery circuitry so as to reduce the extra wiring and external interface connection so that the system reliability can be improved.

All other limitation is contained in claims 11 and 12. The explanation of all the limitation is already addressed in the above paragraph.

Allowable Subject Matter

6. Claims 4, 5, 20, 21, and 27-37are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

7. Reference(s) US 5,329,559 and US 6,324,236 are cited because they are put pertinent to the clock and data recovery scheme with polarized transition phase detector. However, none of references teach detailed connection as recited in claim.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ted M. Wang whose telephone number is 571-272-3053. The examiner can normally be reached on M-F, 7:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on 571-272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ted M Wang
Examiner
Art Unit 2634

Ted M. Wang

KEVIN BURD
PRIMARY EXAMINER